Optimized readout methods of silicon drift detectors for high-resolution X-ray spectroscopy

A. Niculaea,*, P. Lechnera,b, H. Soltua,b, G. Lutzc,b, L. Strüderd,b, C. Fiorinie, A. Longonie

a PNSensor GmbH, Römerstraße 28, 80803 Munich, Germany
b MPI Halbleiterlabor, Otto-Hahn-Ring 6, 81739 Munich, Germany
c Max-Planck-Institut für Physik, 80805 Munich, Germany
d Max-Planck-Institut für extraterrestrische Physik, 85748 Garching, Germany
e Politecnico di Milano, Dipartimento di Elettronica e Informazione, Via Golgi 40, 20133 Milano, Italy

Available online 7 July 2006

Abstract

Silicon Drift Detectors with integrated FET transistor fabricated at Max-Planck-Institute in Munich in cooperation with PNSensor GmbH are widely used as X-ray sensors in many industrial and scientific applications. In the classical readout scheme, the integrated transistor on the SDD is operated in the source–follower configuration. The signal charge is removed continuously by the detector self-rest mechanism. The method gives very good results at counting rates up to 10 kcps. For higher count rates, the FWHM increases with the growing reset current and a slight shift of the energy peak is observed. The relative large signal rise time can be also a limitation for operation at very high count rates. Alternatively, the SDD can be operated in a Charge Sensitive Amplifier (CSA) configuration. The detector signal charge is integrated on a feedback capacitor across an inverting amplifier with the integrated FET as the input transistor. The signal rise time does not depend on the integrated transistor and can be made very short (e.g. 50 ns). In applications requiring very high counting rates and constant energy resolution, pulsed-reset operation of the SDD is desirable. The signal charge is removed by applying short reset pulses to a reset structure integrated on the detector anode. The combination of the CSA readout scheme and the pulsed-reset method allows the operation at the best energy resolution independent on the count rate.

© 2006 Elsevier B.V. All rights reserved.

PACS: 07.85.Fv; 07.50.Qx; 29.30.Kv

Keywords: Drift detectors; SDD; X-ray spectroscopy; SDD readout

1. Introduction

Since their introduction in 1983 [1], Silicon Drift Detectors (SDD) have become very powerful instrumentation tools for industrial and scientific applications in X-ray spectroscopy. Based on the principle of sideward depletion [1], the SDDs combine the advantage of a large sensitive volume with a small capacitance of the readout node and hence, improved noise performances compared to those of a typical PIN diode of the same size. Moreover, the front-end transistor is monolithically integrated [2,3] onto the detector substrate (see Fig. 1) resulting in a minimization the stray capacitance of the readout node and avoiding unwanted interference effects related to wire connections, such as pick-up noise or microphony.

In its classical design, the SDD has a round shape, with the detector anode and the integrated transistor placed in the center of the detector. The detectors exist in sizes of 5, 10, 20 and 30 mm². Besides the classical SDD with a round shape, a novel SDD design has been recently introduced [4]. The detector has a droplet shape, the anode and the integrated FET are moved to the border of the detector area. This new geometry allows on one hand the minimization of the anode area down to the technological limits, i.e. reducing further the total detector capacitance.
(better noise performances at smaller shaping times); on the other hand, the transistor can be covered with a collimator, eliminating the charge loss in the transistor area (i.e. transistor drain is attractive for signal electrons) and reducing partly undesired background events in an X-ray spectrum.

In this paper we present different readout methods of silicon drift detectors with integrated FET, draw attention to their specific applications and report on selected measurement results.

2. SDD readout configurations

2.1. Source–follower readout and self-reset operation

The most frequently used method to operate the SDD with on-chip FET is the source–follower readout [5] with the detector operated in the self-reset mode. As shown in Fig. 2, the integrated JFET is biased in a source–follower configuration and is followed by a voltage amplifier. $C_d$ is the total capacitance seen by the detector anode and is a sum of the gate-drain capacitance $C_{gd}$ and the depletion capacitances between the anode and the neighboring regions—$C_{bulk}$, $C_{a-ig}$, $C_{a-r1}$ in Fig. 3. $C_{gs}$ is the gate-source capacitance of the integrated FET and $C_L$ is the total load capacitance at the source node.

The self-reset mechanism—represented in the circuit by the resistance $R_d$—works basically in the following way: as the electrons (signal or/and thermally generated) are collected to the detector anode, this becomes more and more negative. Consequently the transistor gate gets increasingly reverse biased with respect to the channel. At a given potential difference, a weak avalanche breakdown region is formed in the transistor channel between gate and drain; the holes generated in this region are collected at the gate and compensate for the signal/leakage electrons. A very detailed characterization of the discharging mechanism can be found in Ref. [6].

Performing the small-signal analysis of the circuit in Fig. 2, the expression of the source voltage $v_s(s)$ in frequency domain ($s = j \cdot \omega$) is found to be:

$$v_s(s) = \frac{Q_{in}}{C_d} \left( \frac{1}{1 + \frac{g_m}{g_{ds}}(1 + \frac{C_{gd}}{C_{gs}})} \right) \frac{s \cdot \tau_{f1}}{1 + s / z_0} \left( 1 + s \cdot \tau_r \right)$$  \hspace{1cm} (1)

where $Q_{in}$ is the input charge, $g_m$ and $g_{ds}$ are the transconductance and the channel conductance of the integrated transistor, respectively; $z_0$ is a high-frequency zero given by $z_0 = g_m / C_{gs}$ and plays no role at the frequencies of interest.

Considering the input charge as a time-domain step function, $\tau_r$ is the rise time (the time constant of the exponential increase) of the source signal, whereas $\tau_{f1}$ is the decay time constant of the source signal. They are given by

$$\tau_r = \frac{C_L + C_{in} + \frac{C_{gd}}{\tau_{gd} + \tau_{dp}}}{g_{ds} + g_m \tau_{gd} + \tau_{dp}} \approx \frac{C_L + C_{in}}{g_{ds} + g_m \frac{C_{gd}}{\tau_{gd} + \tau_{dp}}}$$  \hspace{1cm} (2)

$$\tau_{f1} = R_d \cdot \left[ C_d + C_{gs} \cdot \frac{g_{ds}}{g_m + g_{ds}} \right].$$  \hspace{1cm} (3)

Analyzing the expression of $\tau_r$ from Eq. (2), one can see that the amplifier rise time is determined by the total capacitance seen by the source node and the transistor parameters $g_m$ and $g_{ds}$. Since the optimization of the integrated transistor with respect to these parameters is limited by the technology, the minimization of the signal...
rise time is also limited. Typical values of $\tau_r$ are in the range of 80–100 ns for 10 pF total load capacitance.

The output voltage of the whole amplifier chain is given by

$$v_{\text{out}}(s) = -v_s(s) \cdot \frac{C_{\text{in}}}{C_{\text{fb}}} \cdot \frac{s \cdot \tau_2}{1 + s \cdot \tau_2}$$

(4)

where $\tau_2 = C_{\text{fb}} \cdot R_{\text{fb}}$ is the decay time constant of the voltage amplifier.

2.2. Charge sensitive amplifier readout and self-reset operation

The rise time limitations of the source–follower readout configuration can be overcome by choosing an alternative readout scheme of the SDD, which is the charge-sensitive-amplifier (CSA) readout. This readout concept is commonly used for PIN diode detector types (with external front-end transistors) and has also been implemented for some special types of SDD detectors having an integrated feedback capacitor [7,8].

The standard SDDs detectors have no integrated capacitors; nevertheless one can use the parasitic capacitor between the detector anode and the transistor guard ring ($C_{\text{a-ig}}$ in Fig. 3) as feedback capacitor. The circuit schematic is shown in Fig. 4. The integrated transistor is still biased in the source follower configuration, but is followed by a low input impedance, high gain amplifier resulting into a high gain inverting voltage amplifier. The collected charge will be integrated over the feedback capacitor $C_{\text{a-ig}}$. $R_b$ is a very large resistance needed to bias the transistor guard ring with a negative voltage, $C_c$ is a large coupling capacitor needed to decouple the DC voltages of the guard ring and the amplifier output. Their influence in the amplifier transfer function can be neglected.

The frequency transfer function of the CSA readout configuration can be determined by considering some assumptions like ideal operational amplifier $A_0$ with $A_0 \to \infty$ and infinite bandwidth and is given by:

$$v_{\text{out}}(s) \approx \frac{Q_{\text{in}}}{C_{\text{a-ig}}} \cdot \frac{s \cdot \tau_1}{1 + s \cdot \tau_1} \cdot \frac{s \cdot \tau_2}{1 + s \cdot \tau_2}$$

(5)

where

$$\tau_1 = R_d \cdot C_{\text{a-ig}}, \quad \tau_2 = R_{\text{fb}} \cdot C_{\text{in}}.$$  

(6)

The time constants $\tau_1$ and $\tau_2$ are determined with the approximation that $\tau_1 \gg \tau_2$ which is valid since the dynamical resistance $R_d$ is very large (e.g. hundreds of GΩ). One can observe that the frequency bandwidth of the amplifier is no more limited by the integrated transistor parameters $g_m$ and $g_{ds}$. The rise time of the output signal is then determined by the rise time of the incoming charge signal.

3. Pulsed reset operation mode

As described in the previous section, the self-reset operation is a very comfortable way of operating the SDDs. However, the reset current provided by the self-reset mechanism to discharge the anode acts in the same way as the detector leakage current as far as the noise is concerned. Since the reset current is proportional to the input photon rate, it is unavoidable that the energy resolution degrades with the increasing photon rate. For application requiring constant energy resolution over a large range of input count rates, the pulsed reset operation mode can be employed.
To operate the detector in the pulsed reset mode, a reset structure integrated directly onto the detector anode (see Fig. 5) can be used; by applying short positive pulses to this diode, the signal charge collected at the anode is removed.

For the pulsed reset operation of the SDD with integrated FET, the CSA readout configuration shown in Fig. 4 has been employed.

4. Measurements and results

The spectroscopic measurements performed with SDDs operated in the readout configurations described in the previous section will be now presented.

4.1. Source-follower vs. CSA readout

To compare the performance of both SF and the CSA readout configurations, spectroscopic measurements with a conventional 5 mm² SDD operated in the self-reset mode have been carried out. Fig. 6 shows the oscilloscope waveform of the CSA output signal due to a 5.9 keV photon from a $^{55}$Fe radioactive source. The rise time measured from 10% to 90% of the amplitude (i.e. $2.2 \times \tau_r$) is about 50 ns and is much smaller than in the SF readout (e.g. 200–300 ns). From the amplitude of the 5.9 keV signals, a value of about 30 fF has been estimated for the parasitic feedback capacitance $C_{par}$. The energy spectra of the $^{55}$Fe radioactive source measured in both configurations with the detector cooled at $-20^\circ C$ and a shaping time of 1 μs are plotted Fig. 7. The value of the input photon rate was about 1 kcps. As expected, the noise performances are similar in both configurations and this is due to the fact that the noise is determined entirely by detector capacitance, by the leakage current and by the properties of the input transistor integrated on the detector [9].

The energy resolution measured at different input photon rates is plotted in Fig. 8. The operation temperature was again $-20^\circ C$ and the shaping time was reduced to 250 ns in order to minimize pile-up events at high count rates. One can see in both cases the same expected degradation of the energy resolution with the increasing input count rate due to the increase of the reset current in the self-reset mechanism, as previously explained.

Another consequence of the self-reset mechanism, which has not been discussed so far, is the change of the peak position with the changing input count rate, which can be
observed in the plot of Fig. 9. The change is caused by the discharging mechanism which is self-adapting, therefore the reset current sets itself to the values needed to compensate the various rates of signal electrons arriving to the anode. This leads to a change of the anode potential which translates into a change of the depletion capacitances connected to the anode and contributing to the signal amplitude.

Now looking at the expression of the source voltage in Eq. (1), this is inverse proportional to the total capacitance $C_d = C_{g-d} + C_{a-ig} + C_{a-r1} + C_{bulk}$. The initial increase of the peak position can be explained by the reduction of the capacitance $C_{g-d}$ with more negative gate voltage. At the same time, the other capacitances which contributes to $C_d$ increase with the decreasing anode voltage due to the increasing input count rate. Their variation becomes dominant for the last part of the plot.

In the case of the CSA readout, only one capacitance ($C_{a-ig}$) determines the signal amplitude (see Eq. (5)). With more negative anode voltage due to the increase of the count rate, $C_{a-ig}$ increases and the peak position decrease.

In both cases the peak position change with the input rate (or with the temperature) can be greatly reduced by using a peak shift compensation circuit. Using such a circuit, a minimum peak shift of $\pm0.03\%$ (i.e. $\pm2\text{eV}$ for 5.9 keV photons) up to input count rates as high as 400 kcps has been reported in Ref. [10].

4.2. Measurements of the SDDs in pulsed reset mode

As already mentioned, the CSA readout circuit described in Fig. 4 has been used for the measurements with SDDs operated in the pulsed reset mode. The dynamical resistance $R_d$ of the self-reset mechanism must be however replaced by the reset diode connected to the detector anode.
Fig. 10 shows the amplifier output signal recorded on the oscilloscope when a periodic reset pulse is applied to the reset diode. One can observe the well-known ramp shape of the signal with the linear increase due to the charging of the integrated capacitor with the detector leakage current. The light curvature of the signal between the reset pulses is due to the amplifier AC coupling, i.e. the coupling capacitor $C_{\text{in}}$ which gives the finite time constant $\tau_2$ in the amplifier transfer function of Eq. (5).

The amplitude of the voltage step at the amplifier output after the reset pulse ($\Delta V_{\text{out}}$ in Fig. 10) is measured as a function of the reset ON voltage and is plotted in Fig. 11a. One can easily see that the amplitude of the output voltage step reaches its saturation (i.e. complete reset) for reset ON voltages higher than $+5\,\text{V}$ (transistor drain fixed to $+10\,\text{V}$). Fig. 11b shows the amplitude of the output voltage step as a function of the reset pulse width. The complete reset is already achieved for reset pulses as short as $50\,\text{ns}$.

With the reset ON voltage fixed at $+7\,\text{V}$, the reset pulse width of $200\,\text{ns}$ and the reset rate of $1\,\text{kHz}$, spectroscopic measurements with the $5\,\text{mm}^2$ standard SDD cooled at $-20\,\text{°C}$ have been performed. The energy resolution of the Mn-K$_\alpha$ line from the $^{55}\text{Fe}$ spectrum measured as a function of the input count rate at $0.5\,\mu\text{s}$ shaping time is plotted in Fig. 12. For comparison, the energy resolution measured in the self-reset mode under the same conditions (temperature and shaping time) are plotted in the same graph. One can easily see the benefit of the pulsed reset operation: while operated in self-reset mode, the energy resolution increases with about $40\,\text{eV}$ up to $120\,\text{kcps}$ input count rate, the resolution remains almost unchanged ($3-4\,\text{eV}$ increase) when the SDD is operated in pulsed reset mode.

The peak shift with the count rate is also reduced when the pulsed reset operation is employed. Fig. 13 shows the peak position of the Mn-K$_\alpha$ line measured as a function of the input count rate for both self-reset (without peak shift compensation circuit) and pulsed reset detector operation.

The peak shift could be even further reduced if one uses a variable (self-adapting) reset rate, thus increasing the reset rate with the increasing count rate and maintaining fixed variation limits for the voltage across the feedback capacitor.

Measurements in pulsed reset mode of the energy resolution for different input count rates have been carried out also with other SDD types. The results obtained with a $5\,\text{mm}^2$ SD3 detector (droplet shape), a $10\,\text{mm}^2$ PSDD and a $30\,\text{mm}^2$ PSDD detector round shape (PSDDs are drift detectors fabricated in a new technology involving poly-Si) are plotted in Fig. 14. The measurements were done at $-20\,\text{°C}$ and $1\,\mu\text{s}$ shaping time. One can remark the excellent energy resolution of the droplet shape SDD of lower than
128 eV up to 100 kcps input count rate. The performance of the 30 mm$^2$ SDD showing an energy resolution better than 140 eV is also remarkable.

5. Conclusions

Various readout configurations of the SDDs with integrated FET have been presented. Operated in source–follower or in CSA configuration, the detector noise performances are similar as they are entirely determined by the detector capacitance and by the properties of the integrated JFET. The CSA configuration has the advantage of a faster rise time, improving the performances at very high count rates.

The self-reset operation mode is a very convenient way to operate the detector at low and medium input count rates. The degradation of the energy resolution with the increasing input count rate can be beaten by operating the detector in the pulsed reset mode. Energy resolutions below 128 eV have been measured with a 5 mm$^2$ SDD droplet type at $-20^\circ$C and input count rates up to 100 kcps.

References